WHAT IS CLAIMED IS:

1. A method of fabricating a multi-chip module, comprising:
partitioning an integrated circuit design to include a first circuit segment and a second circuit segment, wherein functionality associated the first circuit segment and functionality associated with the second circuit segment jointly enable functionality of the integrated circuit design;
fabricating a first semiconductor device capable of enabling said functionality associated with the first circuit segment and including an array of first device interconnect pads;
fabricating a second semiconductor device capable of enabling said functionality associated with the second circuit segment and including an array of second device interconnect pads; and
facilitating direct interconnection between each one of said first device interconnect pads and a corresponding one of said second device interconnect pads.

2. The method of claim 1 wherein partitioning the integrated circuit design to include a first circuit segment and a second circuit segment includes defining a first functional block of the integrated circuit design and a second functional block of the integrated circuit design.

3. The method of claim 2 wherein defining the first functional block and the second functional block includes defining a memory functional block and a logic functional block, respectively.

4. The method of claim 1 wherein partitioning the integrated circuit design to include a first circuit segment and a second circuit segment includes partitioning the integrated circuit design such that the first circuit segment is associated with a first type of semiconductor substrate and the second circuit segment is associated with a second type of semiconductor substrate.

5. The method of claim 1 wherein partitioning the integrated circuit design to include a first circuit segment and a second circuit segment includes partitioning the integrated circuit design such that the first circuit segment is associated with a first semiconductor fabrication process and the second circuit segment is associated with a second semiconductor fabrication process.

6. The method of claim 1 wherein:

fabricating the first semiconductor device includes fabricating the first semiconductor device for being capable of enabling functionality associated with a first functional block of the integrated circuit design; and

fabricating the second semiconductor device includes fabricating the second semiconductor device for being capable of enabling functionality associated with a second functional block of the integrated circuit design.

7. The method of claim 1 wherein:

fabricating the first semiconductor device includes fabricating a DRAM device; and

fabricating the second semiconductor device includes fabricating a logic device.

8. The method of claim 1 wherein:

fabricating the first semiconductor device includes fabricating the first semiconductor device from a first type of semiconductor substrate; and

fabricating the second semiconductor device includes fabricating the second semiconductor device from a second type of semiconductor substrate.

9. The method of claim 1 wherein:
fabricating the first semiconductor device includes fabricating the first semiconductor device using a first semiconductor fabrication process; and
fabricating the second semiconductor device includes fabricating the second semiconductor device using a second semiconductor fabrication process.

10. The method of claim 1 wherein facilitating direct interconnection between each one of said first device interconnect pads and a corresponding one of said second device interconnect pads includes forming a solder-type interconnect between each one of said first device interconnect pads and the corresponding one of said second device interconnect pads.

11. The method of claim 10 wherein forming the solder-type interconnect includes forming a solder bump interconnect.

12. The method of claim 10 wherein forming the solder-type interconnect includes forming a solderball ball interconnect.

13. A method of fabricating a multi-chip module, comprising:

partitioning an integrated circuit design to include a first functional block and a second functional block, wherein functionality associated the first functional block and functionality associated with the second functional block jointly enable functionality of the integrated circuit design;

fabricating a first semiconductor device capable of enabling said functionality associated with the first functional block and including an array of first device interconnect pads;

fabricating a second semiconductor device capable of enabling said functionality associated with the second functional block and including an array of second device interconnect pads; and

facilitating a solder-type interconnect directly between each one of said first device interconnect pads and a corresponding one of said second device interconnect pads.

14. The method of claim 13 wherein partitioning the integrated circuit design to include the first functional block and the second functional block includes defining a memory functional block and a logic functional block, respectively.

15. The method of claim 13 wherein partitioning the integrated circuit design to include a first functional block and a second functional block includes partitioning the integrated circuit design such that the first functional block is associated with a first type of semiconductor substrate and the second functional block is associated with a second type of semiconductor substrate.

16. The method of claim 13 wherein partitioning the integrated circuit design to include a first circuit functional block and a second functional block includes partitioning the integrated circuit design such that the first functional block is associated with a first semiconductor fabrication process and the second functional block is associated with a second semiconductor fabrication process.

17. The method of claim 13 wherein forming the solder-type interconnect includes forming a solder bump interconnect.

18. The method of claim 13 wherein forming the solder-type interconnect includes forming a solder ball interconnect.

19. A multi-chip module, comprising:

a first semiconductor device capable of enabling functionality associated with a first circuit segment of an integrated circuit design and including an array of first device interconnect pads;

a second semiconductor device capable of enabling functionality associated with a second circuit segment of the integrated circuit design and including an array of second device interconnect pads; and

a plurality of device interconnect members, each one of said device interconnect members being electrically connected directly between one of said first device interconnect pads and a corresponding one of said second device interconnect pads.

20. The multi-chip module of claim 19 wherein:

the first semiconductor device includes is capable of enabling functionality associated with a first functional block of the integrated circuit design; and

the second semiconductor device is capable of enabling functionality associated with a second functional block of the integrated circuit design.

21. The multi-chip module of claim 19 wherein:

the first semiconductor device is a DRAM device; and

the second semiconductor device is a logic device.

22. The multi-chip module of claim 19 wherein:

the first semiconductor device is made from a first type of semiconductor substrate; and

the second semiconductor device is made from a second type of semiconductor substrate.

23. The multi-chip module of claim 19 wherein each one of said device interconnect members is a solder-type interconnect member.

24. The multi-chip module of claim 23 wherein the solder-type interconnect member is a solder bump.

25. The multi-chip module of claim 23 wherein the solder-type interconnect member is a solder ball.

26. A multi-chip module, comprising:
a first semiconductor device capable of enabling functionality associated with a first functional block of an integrated circuit design and including an array of first device interconnect members;
a second semiconductor device capable of enabling functionality associated with a second functional block of the integrated circuit design and including an array of second device interconnect members; and
a plurality of solder-type interconnect members, each one of said solder-type interconnect members being electrically connected directly between one of said first device interconnect members and a corresponding one of said second device interconnect members.

27. The multi-chip module of claim 26 wherein:
the first semiconductor device is a DRAM device; and
the second semiconductor device is a logic device.

28. The multi-chip module of claim 26 wherein:
the first semiconductor device is made from a first type of semiconductor substrate; and
the second semiconductor device is made from a second type of semiconductor substrate.

29. The multi-chip module of claim 26 wherein the solder-type interconnect member is a solder bump.

30. The multi-chip module of claim 26 wherein the solder-type interconnect member is a solder ball.

31. An electronic package, comprising:
an interposer circuit including a dielectric substrate and an array of routing elements attached to the dielectric substrate;
a first semiconductor device capable of enabling functionality associated with a first circuit segment of an integrated circuit design and including an array of first device interconnect pads;
a second semiconductor device capable of enabling functionality associated with a second circuit segment of the integrated circuit design, including an array of second device interconnect pads and including a set of package-level interconnect pads;
a plurality of device interconnect members, each one of said device interconnect members being electrically connected directly between one of the said first device interconnect pads and a corresponding one of said second device interconnect pads; and
a plurality of package-level interconnect members, each one of said package-level interconnect members being electrically connected between one of the said package-level interconnect pads of the second semiconductor device and a corresponding one of said routing elements of the interposer circuit.

32. The electronic package of claim 31 wherein:
the first semiconductor device includes is capable of enabling functionality associated with a first functional block of the integrated circuit design; and
the second semiconductor device is capable of enabling functionality associated with a second functional block of the integrated circuit design.

33. The electronic package of claim 31 wherein:
the first semiconductor device is a DRAM device; and
the second semiconductor device is a logic device.

34. The electronic package of claim 31 wherein:
the first semiconductor device is made from a first type of semiconductor substrate; and
the second semiconductor device is made from a second type of semiconductor substrate.

35. The electronic package of claim 31 wherein each one of said device interconnect members is a solder-type interconnect member.

36. The electronic package of claim 35 wherein the solder-type interconnect member is a solder bump.

37. The electronic package of claim 35 wherein the solder-type interconnect member is a solderball.

38. The electronic package of claim 31 wherein:
the interposer circuit is a flip-chip interposer circuit; and
each one of said package-level interconnect members is a solder-type interconnect member.

39. The electronic package of claim 31 wherein:
the interposer circuit is a wire-bond interposer circuit; and
each one of said package-level interconnect members is a conductive wire.

40. An electronic package, comprising:

an interposer circuit including a dielectric substrate and an array of routing elements attached to the dielectric substrate;

a first semiconductor device capable of enabling functionality associated with a first functional block of an integrated circuit design and including an array of first device interconnect members;

a second semiconductor device capable of enabling functionality associated with a second functional block of the integrated circuit design and including an array of second device interconnect members; and

a plurality of solder-type interconnect members, each one of said solder-type interconnect members being electrically connected directly between one of the said first device interconnect members and a corresponding one of said second device interconnect members; and

a plurality of package-level interconnect members, each one of said package-level interconnect members being electrically connected between one of the said package-level interconnect pads of the second semiconductor device and a corresponding one of said routing elements of the interposer circuit.

41. The electronic package of claim 40 wherein:

the first semiconductor device is a DRAM device; and

the second semiconductor device is a logic device.

42. The electronic package of claim 40 wherein:

the first semiconductor device is made from a first type of semiconductor substrate; and

the second semiconductor device is made from a second type of semiconductor substrate.

43. The electronic package of claim 40 wherein the solder-type interconnect member is a solder bump.

44. The electronic package of claim 40 wherein the solder-type interconnect member is a solder ball.

45. The electronic package of claim 40 wherein:
the interposer circuit is a flip-chip interposer circuit; and
each one of said package-level interconnect members is a solder-type interconnect member.

46. The electronic package of claim 40 wherein:
the interposer circuit is a wire-bond interposer circuit; and
each one of said package-level interconnect members is a conductive wire.